

Velosti N-channel 650V, 20A, 0.15Ω Power MOSFET

Description

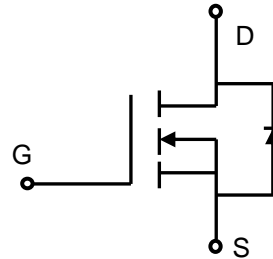
Velosti Power MOSFET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

Features

- ◆ Ultra low $R_{DS(on)}$
- ◆ Ultra low gate charge (typ. $Q_g = 65\text{nC}$)
- ◆ 100% UIS tested
- ◆ RoHS compliant

Product Summary

$V_{DS} @ T_{j,max}$	700V
$R_{DS(on),max}$	0.15Ω
I_{DM}	60A
$Q_{g,typ}$	65nC



N-Channel MOSFET



Absolute Maximum Ratings

Parameter	Symbol	VSQ652015A2	Unit
Drain-Source Voltage	V_{DS}	650	V
Continuous drain current ($T_C = 25^\circ\text{C}$)	I_D	20	A
($T_C = 100^\circ\text{C}$)		13	A
Pulsed drain current ¹⁾	I_{DM}	60	A
Gate-Source voltage	V_{GS}	± 30	V
Avalanche energy, single pulse ²⁾	E_{AS}	700	mJ
Avalanche energy, repetitive ¹⁾	E_{AR}	20.5	mJ
Avalanche current, repetitive ¹⁾	I_{AR}	20	A
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	205	W
- Derate above 25°C		1.64	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Continuous diode forward current	I_S	20	A
Diode pulse current	$I_{S,pulse}$	60	A

Thermal Characteristics

Parameter	Symbol	VSQ652015A2	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.61	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device	Device Package	Marking
VSQ652015A2	TO-220	VSQ652015A2

Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0\text{ V}, I_D=0.25\text{ mA}$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.25\text{ mA}$	2		5	V
Drain cut-off current	I_{DSS}	$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}$,	-	-	1	μA
Gate leakage current, Forward	I_{GSSF}	$V_{GS}=30\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	$V_{GS}=-30\text{ V}, V_{DS}=0\text{ V}$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=10\text{ A}$ $T_j = 25^\circ\text{C}$ $T_j = 150^\circ\text{C}$	- - -	0.13 0.39	0.15 -	Ω
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	1.8	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$,	-	2100	-	pF
Output capacitance	C_{oss}	$f = 1\text{ MHz}$	-	1700	-	
Reverse transfer capacitance	C_{rss}		-	17	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 10\text{ A}$	-	25	-	ns
Rise time	t_r	$R_G = 4.7\Omega, V_{GS}=10\text{ V}$	-	21	-	
Turn-off delay time	$t_{d(off)}$		-	60	-	
Fall time	t_f		-	4	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	$V_{DD}=480\text{ V}, I_D=10\text{ A}$,	-	12	-	nC
Gate to drain charge	Q_{gd}	$V_{GS}=0\text{ to }10\text{ V}$	-	31	-	
Gate charge total	Q_g		-	65	-	
Gate plateau voltage	$V_{plateau}$		-	5.7	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=10\text{ A}$	-	-	1.4	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F=20\text{ A}$,	-	520	-	ns
Reverse recovery charge	Q_{rr}	$di_F/dt=100\text{ A}/\mu\text{s}$	-	5.7	-	μC
Peak reverse recovery current	I_{rrm}		-	19	-	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 7\text{ A}$, $V_{DD} = 60\text{ V}$, $R_G = 25\Omega$, Starting $T_j = 25^\circ\text{C}$

Electrical Characteristics Diagrams

Figure 1. On-Region Characteristics

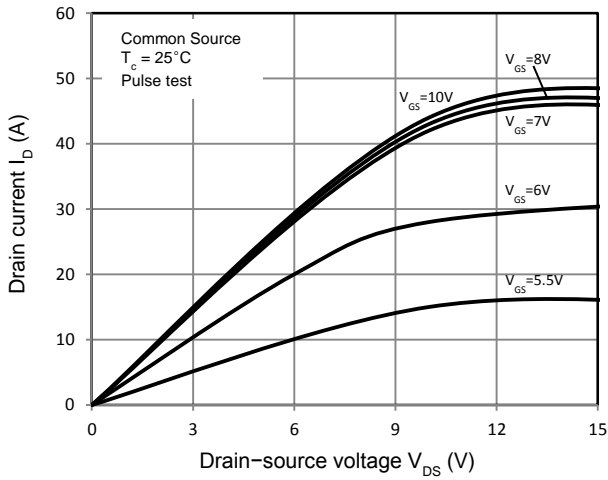


Figure 2. Transfer Characteristics

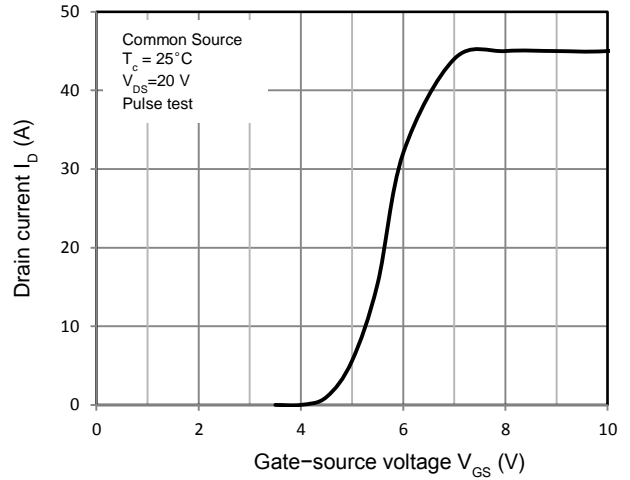


Figure 3. On-Resistance Variation vs. Drain Current

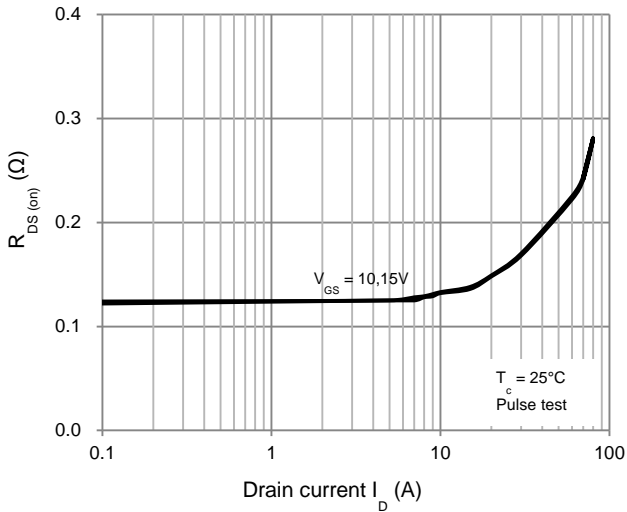


Figure 4. Threshold Voltage vs. Temperature

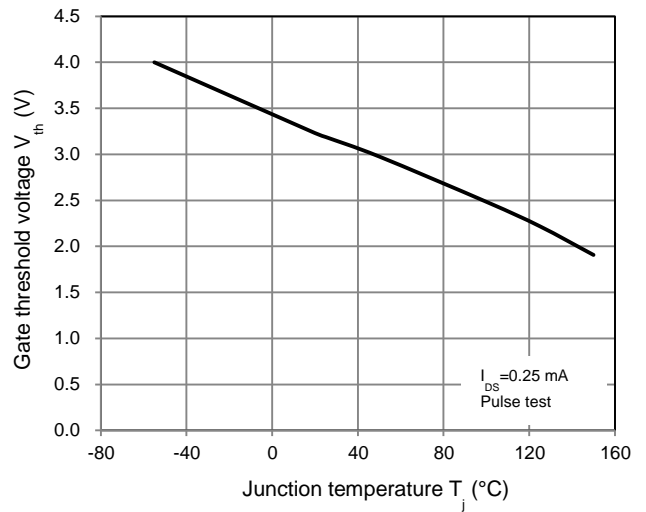


Figure 5. Breakdown Voltage vs. Temperature

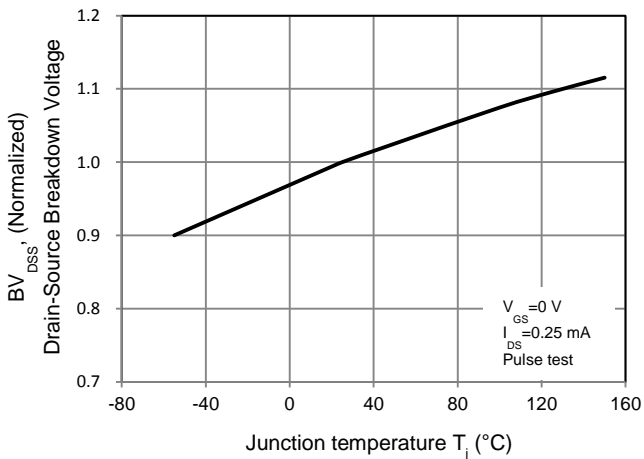


Figure 6. On-Resistance vs. Temperature

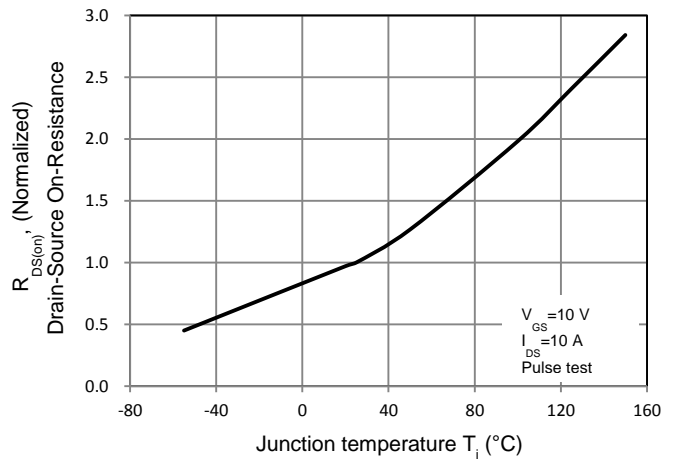


Figure 7. Capacitance Characteristics

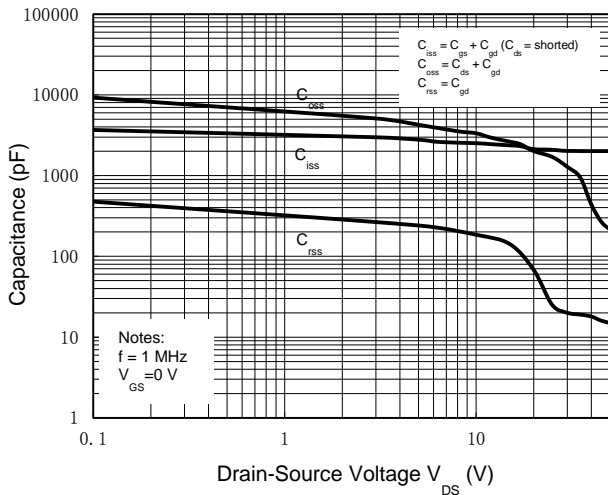


Figure 8. Gate Charge Characteristics

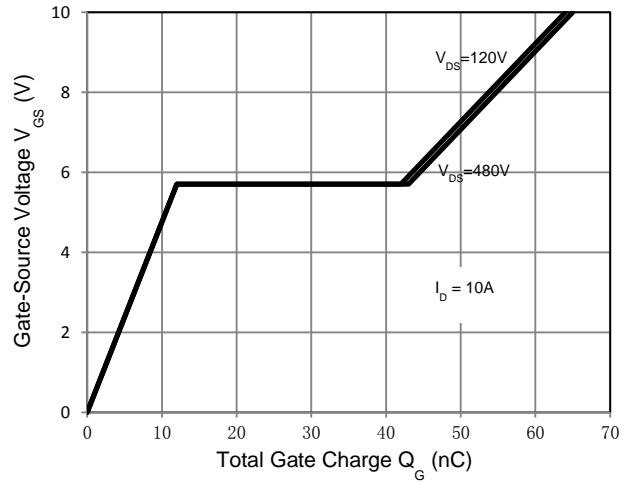


Figure 9. Maximum Safe Operating Area
VSP652015A2, VSQ652015A2

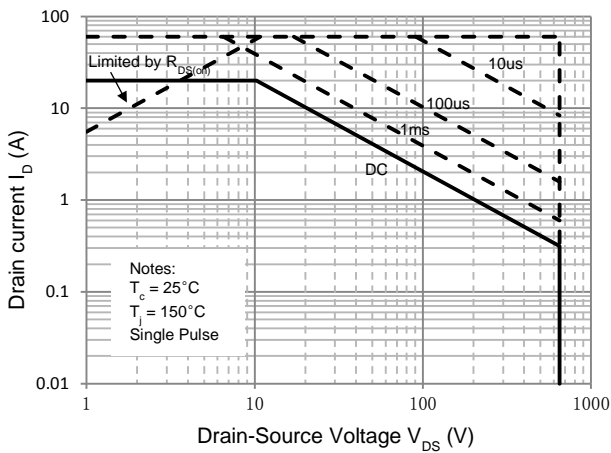


Figure 10. Power Dissipation vs. Temperature
VSP652015A2, VSQ652015A2

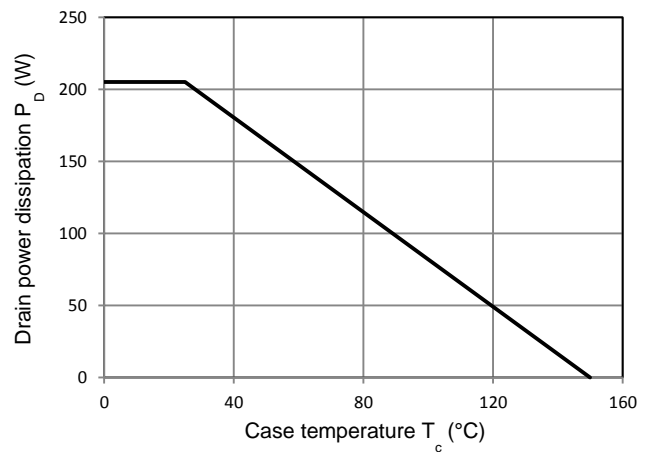
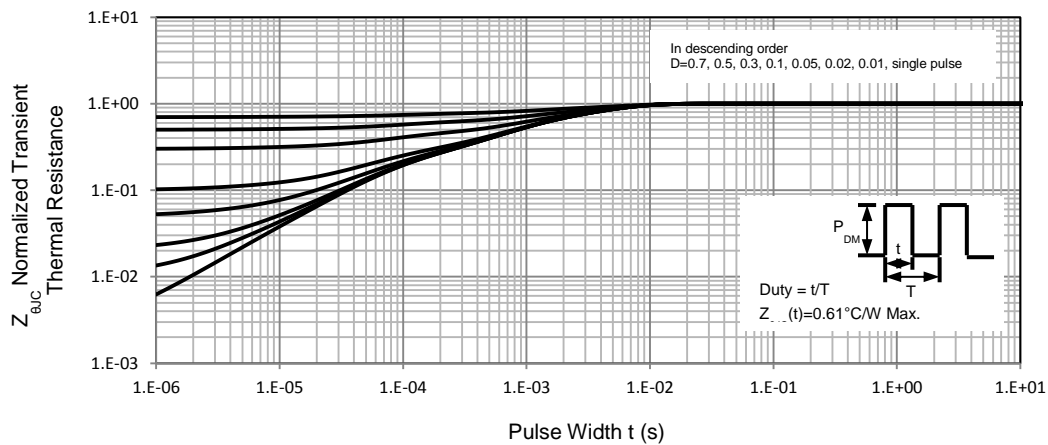
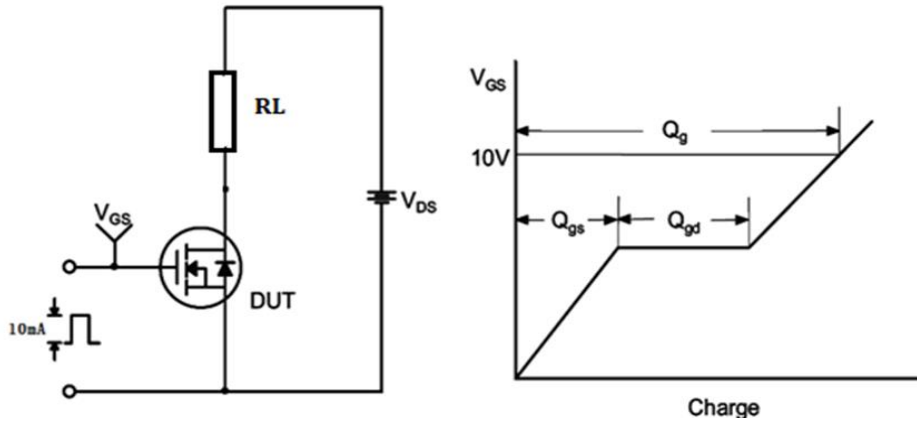


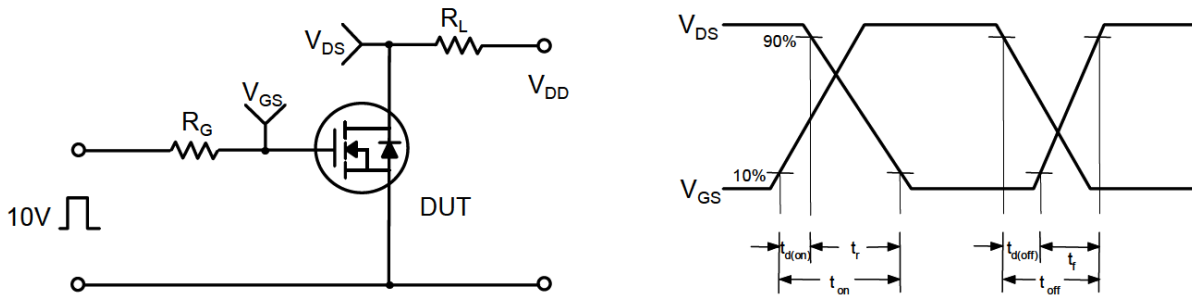
Figure 11. Transient Thermal Response Curve
VSP652015A2, VSQ652015A2



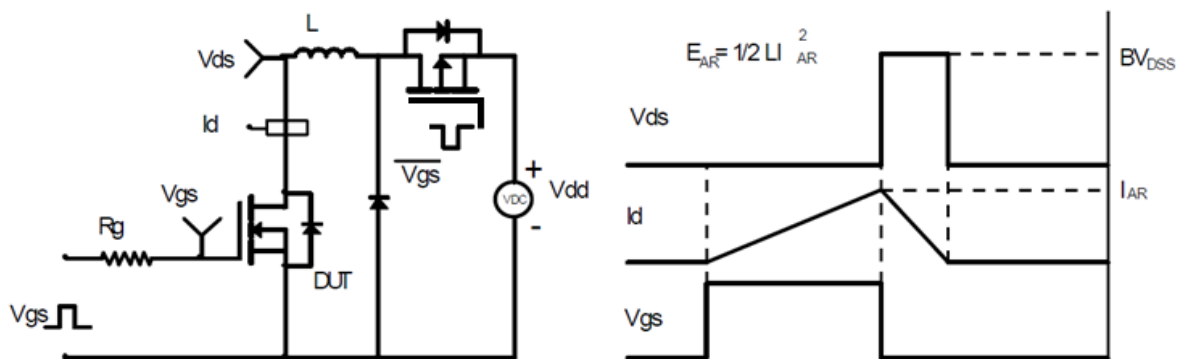
Gate Charge Test Circuit & Waveform



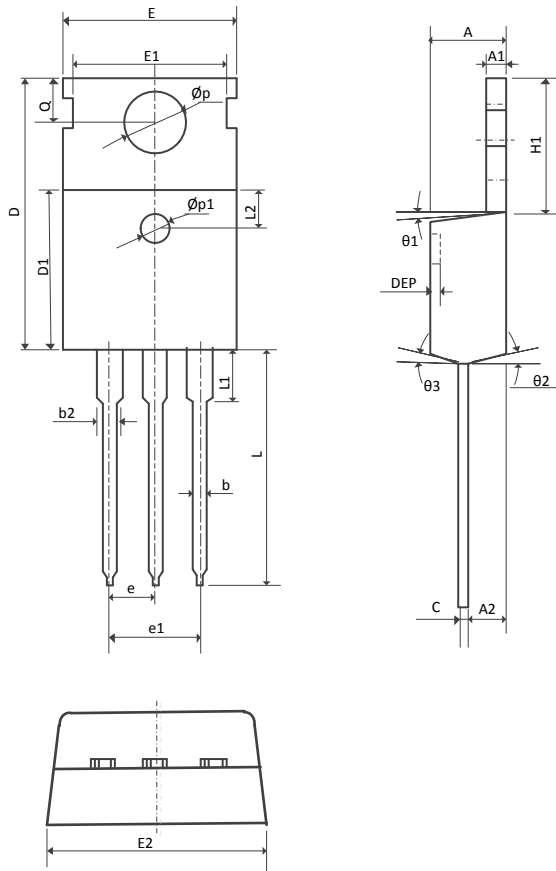
Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions for TO-220



COMMON DIMENSIONS						
SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.37	0.050	0.051	0.054
A2	2.35	2.40	2.50	0.091	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.401
Øp1	1.40	1.50	1.60	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50REF			0.098REF	
Øp	3.50	3.60	3.63	0.137	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.116
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
θ3	1°	3°	5°	1°	3°	5°

Revision History

Date	Revision	Changes
2012-5-9	2.0	First release
2012-12-10	2.1	Updated page header
2013-1-9	2.2	Fixed display error in Mac OS environment
2013-10-25	2.3	Updated the parameters of turn on/turn off, Qg, Qg chart and test condition
2013-11-6	2.4	Revised label marks of figure 4-6
2013-11-22	2.5	Changed label T_c to T_j in figure 4-6. Unified the display format of $R_{DS(on)}$.