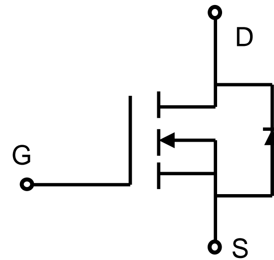
Velosti N-channel 650V, 1A, 5.3Ω Power MOSFET

Description

Velosti Power MOSFET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

Product Summary

V_{DS} @ $T_{j,max}$	700V
$R_{DS(on),max}$	5.3Ω
I_{DM}	2A
$Q_{g,typ}$	5.5nC



N-Channel MOSFET

Features

- Ultra low $R_{DS(on)}$
- Ultra low gate charge (typ. Q_g = 5.5nC)
- Low C_{rss} (typ. 1.4 pF)
- 100% UIS tested
- RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	VSV65R530B2	Unit
Drain-Source Voltage	V_{DS}	650	V
Continuous drain current (T_C = 25°C)	I_D	1	A
(T_C = 100°C)		0.6	A
Pulsed drain current [1]	I_{DM}	2	A
Gate-Source voltage	V_{GS}	±30	V
Avalanche energy, single pulse [2]	E_{AS}	20	mJ
Avalanche energy, repetitive [1]	E_{AR}	0.01	mJ
Avalanche current, repetitive [1]	I_{AR}	1	A
Power Dissipation (T_C = 25°C)	P_D	11	W
- Derate above 25°C		0.09	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	1	A
Diode pulse current	$I_{S,pulse}$	2	A

Thermal Characteristics

Parameter	Symbol	VSV65R530B2	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	11	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	75	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking
VSV65R530B2	TO-252	VSV65R530B2

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	2.5	3.5	4.5	V
Drain cut-off current	I_{DSS}	V_{DS}=650 V, V_{GS}=0 V, T_j = 25°C	-	-	1	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=0.5 A	-			Ω
		T_j = 25°C	-	4.7	5.3	
		T_j = 150°C	-	11.3	-	
Gate resistance	R_G	f=1 MHz, open drain	-	4.5	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	96	-	pF
Output capacitance	C_{oss}		-	62	-	
Reverse transfer capacitance	C_{rss}		-	1.4	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 300V, I_D = 0.5A R_G = 25Ω, V_{GS}=10V	-	11	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	26	-	
Fall time	t_f		-	28	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=480 V, I_D=0.5A, V_{GS}=0 to 10 V	-	0.8	-	nC
Gate to drain charge	Q_{gd}		-	3.7	-	
Gate charge total	Q_g		-	5.5	-	
Gate plateau voltage	$V_{plateau}$		-	5.9	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=0.5A	-	-	1.2	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=1A, dI_F/dt=100 A/μs	-	120	-	ns
Reverse recovery charge	Q_{rr}		-	0.3	-	μC
Peak reverse recovery current	I_{rrm}		-	5	-	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 0.8A, V_{DD} = 60V, R_G = 25Ω, Starting T_J = 25°C

Electrical Characteristics Diagrams

Figure 1. On-Region Characteristics

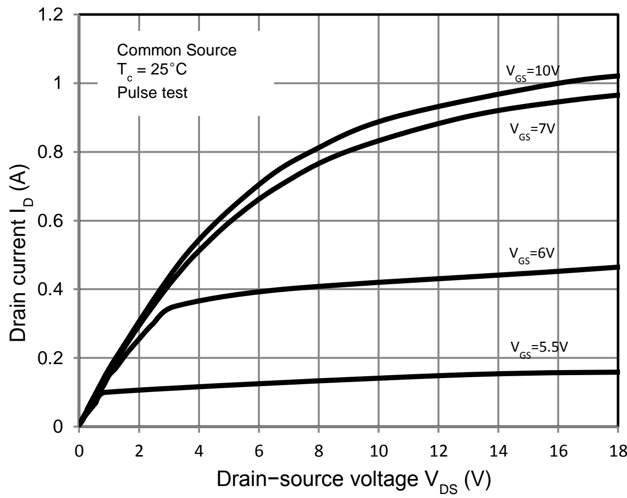


Figure 2. Transfer Characteristics

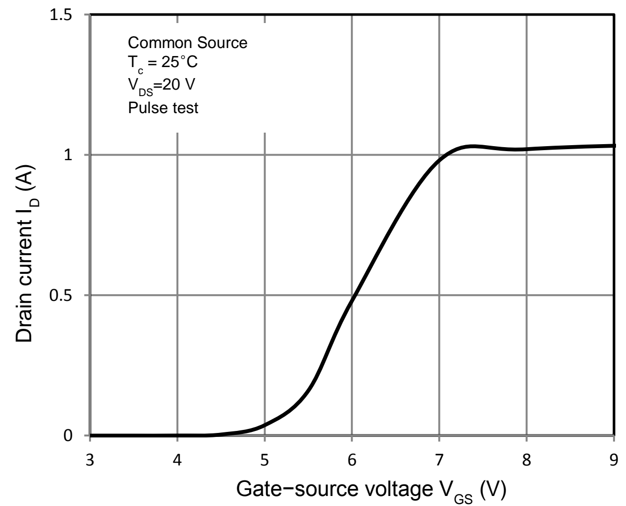


Figure 3. On-Resistance Variation vs. Drain Current

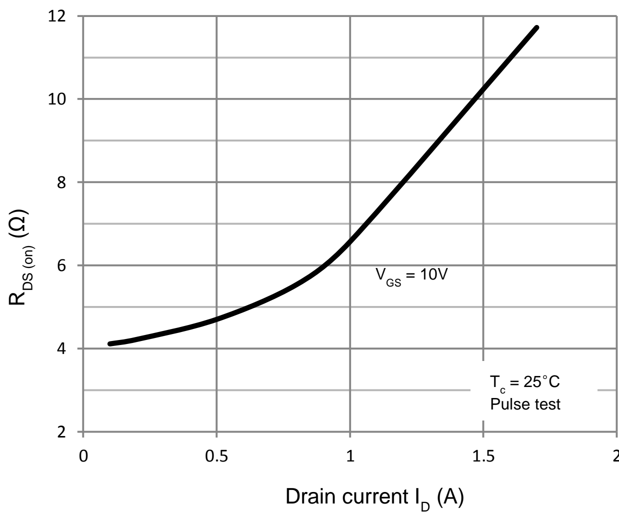


Figure 4. Threshold Voltage vs. Temperature

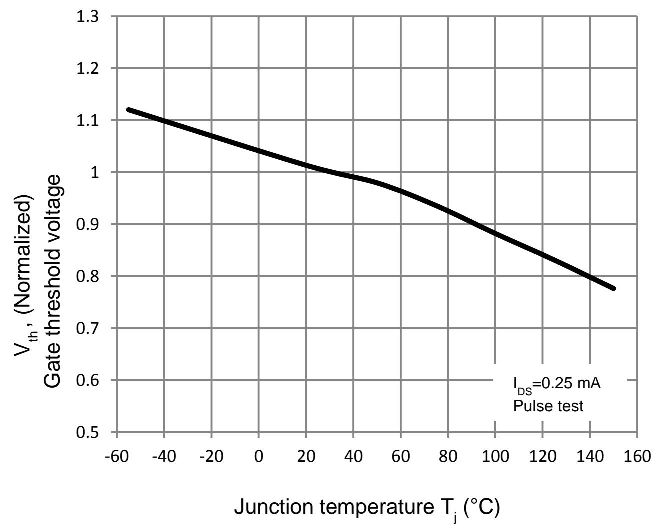


Figure 5. Breakdown Voltage vs. Temperature

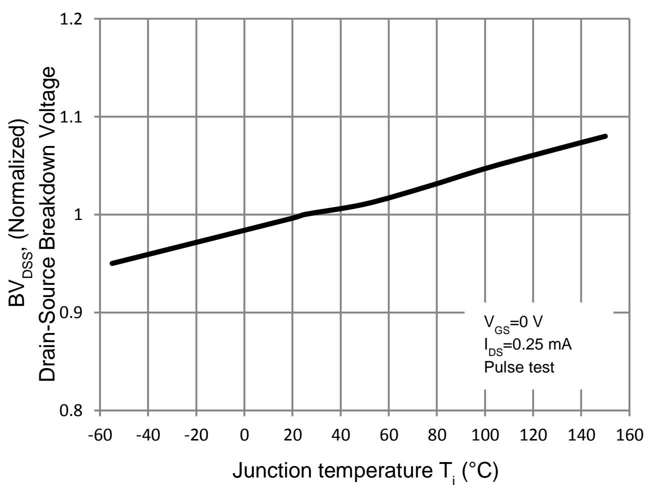


Figure 6. On-Resistance vs. Temperature

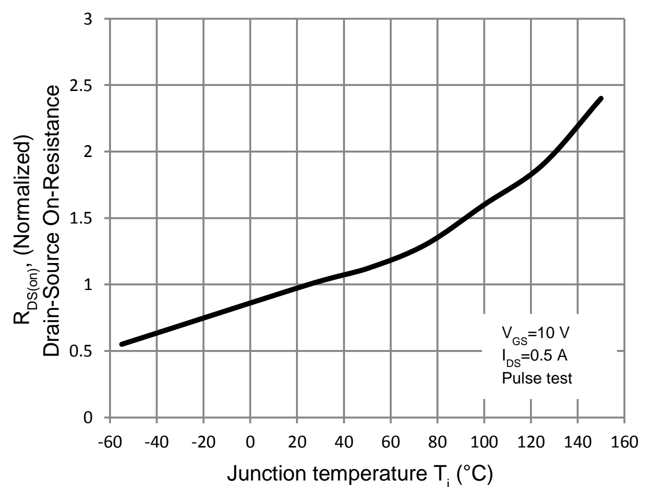


Figure 7. Capacitance Characteristics

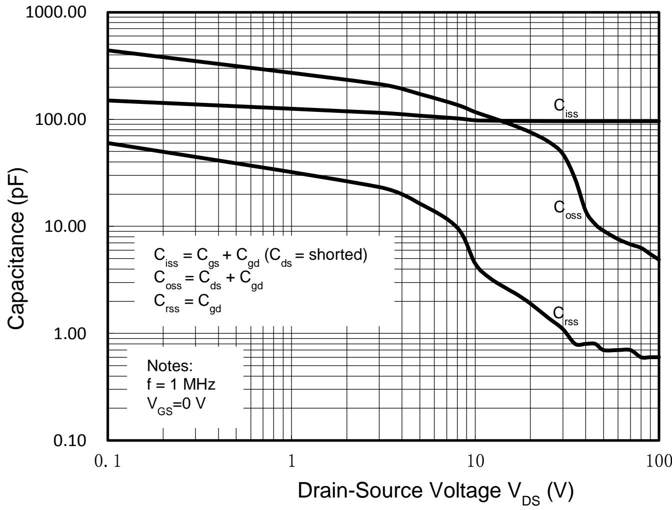


Figure 8. Gate Charge Characteristics

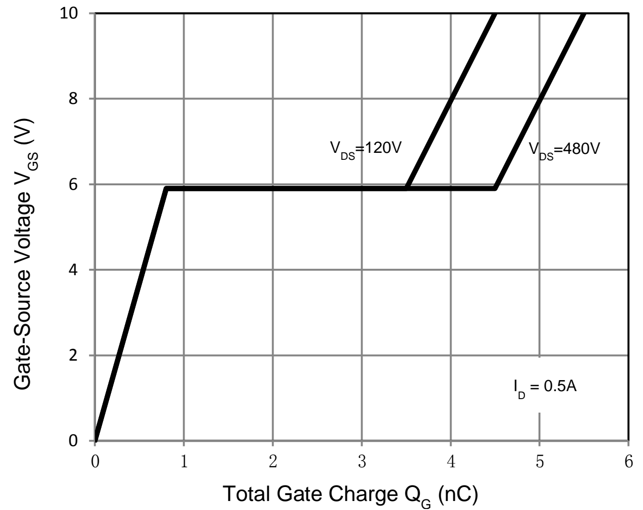


Figure 9. Maximum Safe Operating Area

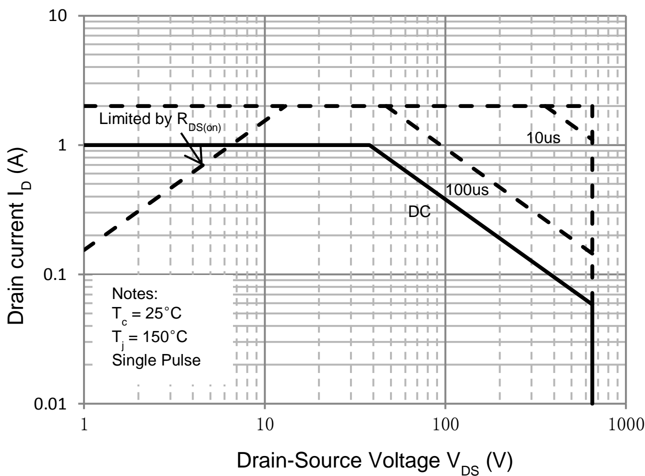


Figure 10. Power Dissipation vs. Temperature

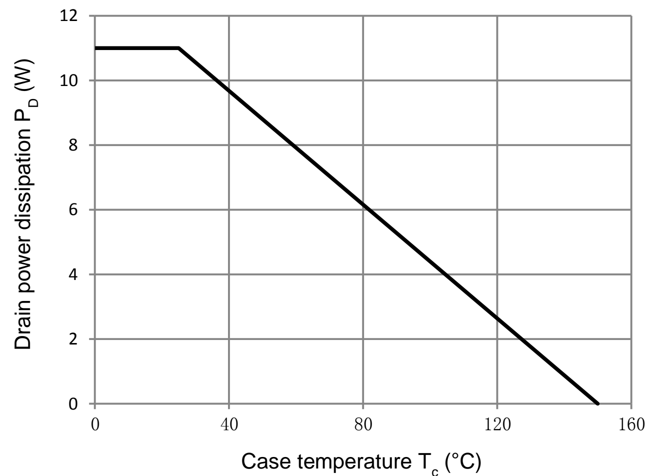
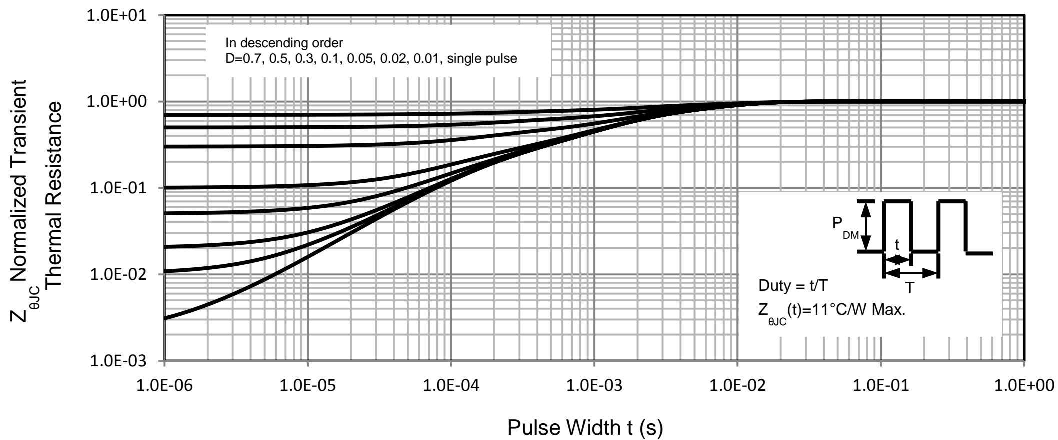
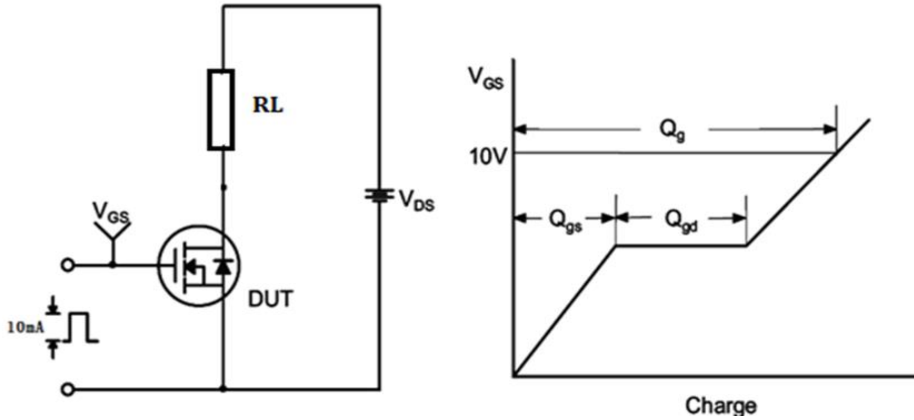


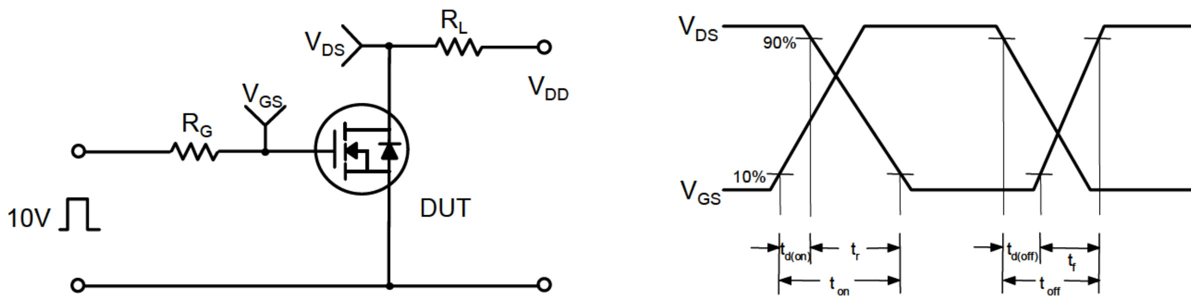
Figure 11. Transient Thermal Response Curve



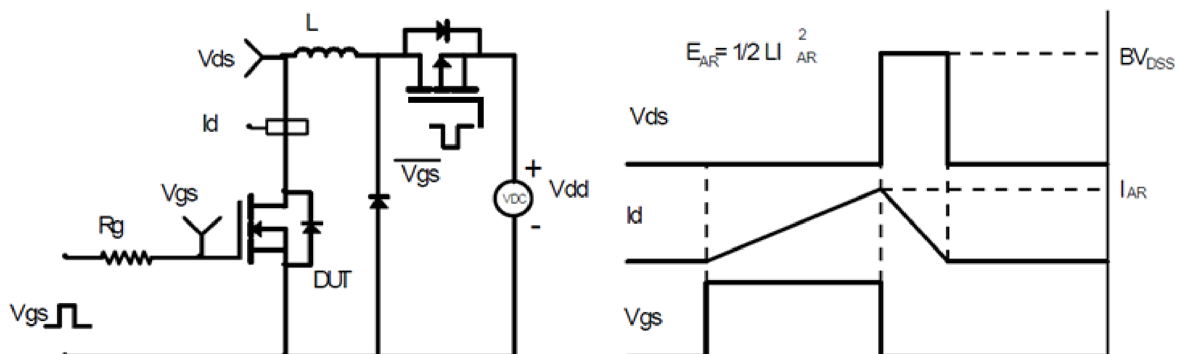
Gate Charge Test Circuit & Waveform



Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions for TO-252

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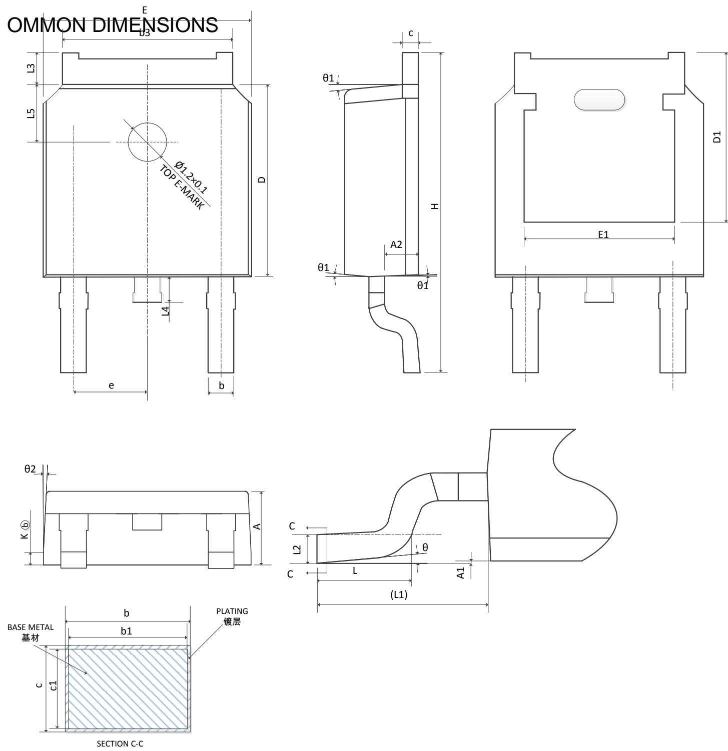

C

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	—	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	—	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	—	8°
θ1	5°	7°	9°
θ2	5°	7°	9°
K	0.40REF		

Revision History

Date	Revision	Changes
2012-5-9	2.0	First release
2012-12-10	2.1	Updated page header
2013-1-9	2.2	Fixed display error in Mac OS environment
2013-11-6	2.3	Revised label marks of figure 4-6.
2013-11-22	2.4	Changed label T_c to T_j in figure 4-6. Unified the display format of $R_{DS(on)}$.